The effect of annealing in forming gas on the a-IGZO thin film transistor performance and valence band cut-off of IGZO on SiNx

Raj Kamal a, Piyush Chandravanshi a, Duck-Kyun Choi b, Santosh M. Bobade c,∗

a Department of Electronics & Communication, Jaypee University of Engineering & Technology, Raghogarh, Guna, Madya Pradesh, India
b Division of Materials Science and Engineering, Haengdang-dong 17, Seoungdong-Ku, Seoul, South Korea
c Department of Physics, Jaypee University of Engineering & Technology, Raghogarh, Guna, Madya Pradesh, India

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In this investigation, the carrier concentration gradient between channel and contact region is achieved to improve the Thin film Transistors (TFT) performance by employing annealing at 350 °C in forming gas (N2 + 5% H2). The contact region is covered with Mo metal and the channel region is only exposed to forming gas to facilitate the diffusion controlled reaction. The TFT using a-IGZO active layer is fabricated in ambient of Ar:O2 in ratio 60:40 and the conductivity of the order of 10−3 S/cm is measured for as deposited sample. The electrical conductivity of an annealed sample is of the order of 102 S/cm. The device performance is determined by measuring merit factors of TFT. The saturation mobility of magnitude 18.5 cm2V−1 s−1 has been determined for W/L (20/10) device at 15 V drain bias. The extrapolated field effect mobility for a device with channel width (W) 10 μm is 19.3 cm2V−1 s−1. The on/off current ratio is 109 and threshold voltage is in the range between 2 and 3 V. The role of annealing on the electronic property of a-IGZO is carried out using X-ray photoelectron spectroscopy (XPS). The valence band cut-off has been approximately shifted to higher binding energy by 1 eV relative to as-deposited sample.

1. Introduction
Recently, Hosono et al. and H.-H. Hsu et al. have demonstrated the use of IGZO for the flexible display [1,2]. The applicability and ease of fabricating a-IGZO at room temperature has attracted attention of many researchers. Several studies have been carried out to improve the performance of TFT. The field effect mobility in various range between 10 and 68.5 cm2V−1 s−1 has been reported by several authors [2–17]. The various experimental conditions such as RF power and co-sputtering [5,10,18], oxygen partial pressure during deposition [12,19], gate oxides [1–6,9,11–14], annealing [20–23], substrate types [5,6,24] and device dimension [5–9,15,16,25–27] have been exploited to improve the performance of TFT. It is to be realized that the field effect mobility has been controlled by varying oxygen’s partial pressure during deposition in almost all the studies.

The device dimensions, are another important parameter that needs to be considered as it plays an important role in improving the resolution of display. In many of the reported investigations, the dimensions are too big [5–8]. To improve it, short channel devices have been demonstrated. However, the variation in the field effect mobility is marginal [9,15,16]. Kim et al. has reported a noticeable performance for small dimensional device. The high mobility of the magnitude of 35.8 cm2V−1 s−1 has been reported for W/L (10/50) μm in [3]. However, the additional process step to form etch stopper has been employed to improve the characteristics. The highest field effect mobility of the magnitude of 68.5 cm2V−1 s−1 has been reported for a-IGZO TFTs using the SiOx passivation and thermal-annealing treatment [10].

The performance of TFT has also been measured in term of saturation mobility as well. Moreover, the saturation mobility has been observed to be significantly smaller than the field effect mobility [28]. The saturation mobility in the range between 1 and 26.66 cm2V−1 s−1 has been determined in various studies [28–34].

Summarizing the reported literature, reasonably good performance has been obtained for extremely higher channel length and width of TFT. Few exceptional studies have been carried out for a small dimensional device including short channel devices as well. The channel length of 6 μm, 10 μm and 50 nm devices have also
been demonstrated in [9,15,16]. However, in those investigation, the field effect mobility exhibits in the range between 7 and 12 cm² V⁻¹ s⁻¹. The high field effect mobility has been obtained for device using etch stopper of SiO₂ [3], which is due to additional process step in fabrication. Although, device dimension is relatively smaller, additional of process makes it unattractive. Thus, it is very beneficial to establish a simple process to fabricate a TFT with good performance. In this investigation, there is no addition of step, such as forming a etch stopper. It is very simple and usual process. The channel region carrier concentration is exclusively altered by annealing in forming gas and device dimension is still small. In presence of some important literature, the effect of annealing in forming gas ambient on electrical performance of a-IGZO TFT and valance band alignment on SiNx along with mechanism has yet to be studied.

In this study, the high performance transistor with very good saturation mobility, the on/off current ratio, and reasonable sub threshold swing for relatively smaller devices are proposed. The fabrication by usual process and control carrier concentration by post annealing are examined.

2. Experimental

The devices were fabricated on glass with dimensions 25 × 25 mm² using usual lithography process. The gate electrode of Mo (100 nm) was deposited using DC magnetron sputter and later was patterned out with channel width of 10, 20, 50 and 100 μm and length 10 μm followed by SiNx deposition at 300 °C using Plasma Enhanced Chemical Vapour Deposition (PECVD). The active layer of a-IGZO of 50 nm was deposited using 80 W RF power. The ambient of Ar:O₂ in the ratio of 60:40 was maintained at 5mTorr working pressure. For forming drain and source, 100 nm Mo was again deposited using DC magnetron sputtering and the electrodes were formed using wet etching process. The device was then annealed at 350 °C for an hour in forming gas (N₂ + 5%H₂) ambient. The transfer characteristics were measured using main frame semiconductor analyzer E5270B. The four probe conductivity measurements at room temperature of as-deposited and annealed samples were carried out. The valance band spectra for both the sample were measured using XPS. The valance band spectra for three different a-IGZO thicknesses on SiNx 200 nm thick layer were also recorded.

The variation in the concentration of different cations between as-deposited and annealed sample suggests that the carrier concentration can be different in channel region and Source/Drain (S/D) region, as S/D is covered by 100 nm thick Mo and 20 μm in width. The ratio of concentration for various cations is provided in Table 1.

In Table 1, the concentration of Ga/Zn is shown. Ga/Zn is the ratio of Ga and Zn in the samples. The concentration is determined in the range between 7 × 10¹⁹ cm⁻³ and 1 × 10¹⁹ cm⁻³. The concentration of Ga/Zn is determined using XPS analysis. However, the IGZO thickness has been suggested that O₂p band in UPS spectra appears in energy range 3 eV–10 eV. However due to lower cross-sectional area, these peaks may not be seen in XPS spectra. On the other hand XPS peak for vacancy appears in spectra [35–37]. Thus, the shift in valence band cut-off seems to be due to the charged oxygen and vacancy at oxygen site which results in the mid gap energy level which is visible in XPS spectra. On annealing, the unreacted oxygen or trap density decrease and the band cut-off shifted to the value of bulk IGZO. The variation in the valence band cut-off with different channel thickness is observed for as-deposited samples as shown in Fig. 3(b). The dependence of complete valence band formation on a-IGZO thickness was being investigated. However, no clear trend has been seen. The valence band of IGZO is built of oxygen and hence spectra for O (1s) peak has been analyzed for all the four samples. The reference of C (1s peak at 284.6 eV) is provided as inset in Fig. 4(a). The detail spectra for O (1s) for as-deposited 7, 21 and 50 nm a-IGZO and the sample 50 nm a-IGZO on annealing are provided in Fig. 4(a, b and c). The two distinct peaks have been observed for all the samples. Although, for the case of 50 nm samples, the ΔBE is equal to 1.6 eV, the nature of peak on annealing is distinguishable. These two peaks in case of ICZO can be attributed two kinds of oxygen surrounding. The higher binding energy peak attributed to (Ga/Zn)–O binding [38], while the lower binding energy peak is associated with In–O binding [39].

The four probe conductivity of a-IGZO on annealing in air and in reducing ambient are observed 3 × 10⁻³ S/cm and 5 × 10⁻² S/cm, respectively. The defect reaction as shown in Eq. (1) occurs in reducing ambient leading to higher carrier concentration.

\[
O^+ = \frac{1}{2} O_2 + V^- + 2e^-
\]  

Further, the electron mobility is also a function of carrier concentration. The fabricated devices have also been annealed in forming gas ambient. The active region of TFT is L + 40 μm leaving

![Fig. 1. Schematic with dimension of exposed area to ambient for annealing the fabricated bottom gate transistor.](image)
20 μm on both sides covered by 100 nm thick Mo contacts. The channel region only exposed to ambient while other part of active region is covered by 100 nm Mo. The schematic of TFT device is already provided in Fig. 1. Thus, the annealing can possibly alter the carrier concentration in channel region. Secondly, Ga/Zn ratio and In/In$^+$Ga$^+$Zn ratio also exhibits variation on annealing. As described, the covered area is less likely to lose oxygen relative to exposed area; the gradient of carrier concentration is likely to exist. The conductivity difference of the order of 5 has been observed for the samples prepared using identical condition but annealed in two different ambient. The sample which has been annealed in reducing ambient exhibits very high conductivity. Considering the scattering of carrier when charge carrier concentration is high, the increase in the mobility that can change the conductivity has been ruled out. Thus, the only suitable reasoning to explain the increase in conductivity is the increase in charge carrier concentration. The loss of oxygen from the IGZO can be compensated by increase in electron concentration.

It has also been reported that the forming gas annealing increases the Hall mobility of GZO film [40]. Hall mobility of the sample in forming gas is higher than that for the as-deposited, annealed in N$_2$ ambient and O$_2$ ambient. Identical argument has been extended to explain the effect of thermal annealing on IGZO.

The electrical performance of fabricated device is discussed in following text. As-fabricated device have not shown switching characteristic. The devices annealed in forming gas exhibit excellent transfer curve and are analyzed below. The saturation mobility and other performance factors of TFT has also been obtained from square law as shown in Eq. (2),

$$I_d = W \frac{L \mu_{FE} \varepsilon_0 (V_{GS} - V_{th})^2}{2d^2}$$

where, $W$ and $L$ are channel width and length and $d$ is thickness of gate insulator, respectively, $\varepsilon$ and $\varepsilon_0$ are permittivity of gate insulator and free space, $\mu_{FE}$ is the mobility and $V_{th}$ is threshold voltage.

The sub threshold swing is extracted using Eq. (3),

$$S = \left( \frac{dV_{GS}}{d\log(I_{DS})} \right)$$

The density of interface trap are extracted from the Eq. (4) given below [13].

$$N_t = \left[ \frac{S \log(e) - 1}{kT/q} \right] \frac{C_i}{q^2}$$

The $I_{DS}$-$V_{GS}$ curves for devices for various channel width, representative $I_{DS}$-$V_{GS}$ for W/L (100 μm/10 μm), are shown in Fig 5 (a–b). The on/off current ratio determined is in the range of $10^8$ to $10^9$. The off and on current has been chosen at −5 V and 30 V gate
bias respectively.

The transfer curve at 5 V drain bias shows marginal threshold voltage variation in the range between 3 and 4 V while the sub-threshold swing decreases with channel width. Further, from the transfer curve for device with 100 μm/10 μm device, the threshold voltage appears to be decreasing with applied drain bias. This kind of behavior is undesired. The drain induced barrier lowering (DIBL) effect is prominent. In case of MOSFET, it is observed for shorter channel length. Shorter the channel length more the drain voltage modulates the source and substrate (a-IGZO) barrier. The off current is also increasing as drain bias increases.

The saturation mobility obtained using Eq. (2) are plotted as a function of channel width in Fig. 6. The saturation mobility exhibits decreasing trend with channel width. The field effect mobility induced by trans-conductance increase with channel length and it has been suggested that contact resistance plays a role [3]. The reported saturation mobility has been lower than that of field effect mobility. The difference in the saturation mobility and trans-conductance induced field effect mobility is approximately 4 times for IGZO TFT [28]. In the reported literature, the trans-conductance induced filed effect mobility is in the range between 10 and 35.8 (cm² V⁻¹ s⁻¹) has been reported [3,5–9,11–17]. However, saturation mobility cannot directly be compare with filed effect mobility. The saturation mobility of about 18.5 cm² V⁻¹ s⁻¹ is still a higher than most of the reported values [28,30,31,33].

The drift component of the drain current is given by
The field effect mobility can be obtained using Eq. (6)

\[ \mu_{	ext{FE}} = \frac{L_{\text{gm}}}{W C_{\text{ox}}} V_{DS} \]  

Sometimes, for a device, \( I_D - V_D \) curves are used for calculating mobility. The drain current for device in saturation can be obtained using Eq. (7)

\[ I_{D,\text{sat}} = \frac{B W \mu_n C_{\text{ox}} (V_{GS} - V_T)^2}{2L} \]  

where \( B \) is the body effect, and is usually assumed to be unity. The mobility obtained using Eq. (7) which is considered as saturation mobility is shown in Eq. (8)

\[ \mu_{\text{sat}} = \frac{2L m^2}{B W C_{\text{ox}}} \]  

where \( m \) is the slope of the \( \ln(I_D) \) versus \( (V_{GS} - V_T) \) plot. The saturation mobility value obtained from Eq. (8) is usually lower than \( \mu_{\text{eff}} \) because the gate voltage dependence of the mobility is neglected in the Eq. (8). The saturation mobility is only valid when the drain current is governed by mobility, not by velocity saturation [41]. Further, it has been suggested that the electron mobility decreases with the increase in carrier concentration. In this case, more carrier concentration is expected in the accumulation region with increase in the gate voltage. Similar argument [42] can be extended to explain the decrease in saturation mobility.

The maximum saturation mobility of the magnitude of 18.5 cm² V⁻¹ s⁻¹ has been observed for the device with 20/10 μm. As channel width increases, the saturation mobility decrease and for \( W/L \) (100/10) μm device it is reduced by 10%. It has been suggested that the spread of channel width and length leads to over estimation of mobility [16]. However, the change in the saturation mobility with channel width (W) using \( V_{DS} = 15 \) V is insignificant. Thus, the contribution of fringing current seems to be less. The variation in mobility as a function of channel width suggests that the contact resistance is increasing with channel width. Secondly, the conductivity of IGZO on annealing in air ambient is \( 10^5 \) times lower than that for the sample annealed in forming gas ambient. As provided in Fig. 1, the covered area by 100 nm Mo blocks the ambient. Thus it can be assumed that the conductivity of contact area is much lower and spreading channel laterally can be insignificant.

The device merit factor as a function of channel width at various applied drain bias are shown in Fig. 7 (a) and (b). Considering the merit factor, the device performance is excellent. The threshold voltage for at \( V_{DS} = 5 \) V is in the range between 3 and 4 V for all the devices. The on/off current ratio varies in the range between \( 10^8 \) and \( 10^9 \). The off current is approximately \( 10^{-13} \) A. The performance of TFT and DIBL effect suggests that short channel effect is responsible for such behavior.

Fig. 6. Saturation mobility as a function of channel width (W) at 15 V drain bias, inset shows saturation mobility for drain bias 5, 10 and 15 V.

\[ I_d = \frac{W_{\text{eff}} C_{\text{ox}}}{L} (V_{GS} - V_T) V_{DS} \]  

\[ \mu_{\text{FE}} = \frac{L_{\text{gm}}}{W C_{\text{ox}}} V_{DS} \]  

\[ I_{D,\text{sat}} = \frac{B W \mu_n C_{\text{ox}} (V_{GS} - V_T)^2}{2L} \]  

\[ \mu_{\text{sat}} = \frac{2L m^2}{B W C_{\text{ox}}} \]  

4. Conclusions

The effect of forming gas annealing on device performance has been demonstrated. Controlling the carrier concentration by post annealing can be achieved by annealing time and temperature. Thermal annealing seems to be required for band structure formation in a-IGZO. The annealing also exhibits variation in atomic concentration which possibly seems to contributing by evaporating unreacted metallic species. The high performance transistor with reasonably high saturation mobility by creating carrier concentration gradient across channel and contact has been demonstrated.

Fig. 7. Device merit factors a function of channel width and various drain bias (a) threshold voltage and off current as a function of channel width (b) the variation of on/off current ratio and sub-threshold swing with channel width.
References