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Highlight

1. Al/HfO$_2$/Au nc/SiO$_2$/Si NFGM MOSCAP structure was studied.
2. Multi-level storage through a stepped control oxide (HfO$_2$) was attempted.
3. Multi-level characteristics were confirmed by C-V measurement.
4. Memory window and trap voltages were predicted by theoretical calculation.
5. The major device parameters were consistent with the predicted values.
Design of control oxide thickness for multi-level storage in a stepped NFGM MOSCAP

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Abstract — In this work, the effect of control oxide thickness on the storage characteristic of MOSCAP based on nano floating gate memory (NFGM) structure was explored in order to apply the results to a stepped NFGM. A stepped MOSCAP structure can realize multi-level storage characteristic via control of electric field strength in the tunneling oxide using a stepped control oxide. Through simulation, we have predicted that a 20nm step height is optimal to exhibit multi-level storage behavior for a 40nm thick HfO\textsubscript{2} control oxide. First, we prepared two step-free NFGM MOSCAP structures consisting of Au nanocrystals: one with 20nm thick HfO\textsubscript{2} control oxide and the other with 40nm thick HfO\textsubscript{2} control oxide. The C-V behavior of NFGM MOSCAP structures having different control oxide thicknesses was measured in a parallel mode in order to simulate the stepped MOSCAP structure. Finally a stepped NFGM MOSCAP stricture was fabricated. As a consequence, we successfully demonstrated multi-level storage behavior in an NFGM MOSCAP structure with 40/20nm step-shape control oxide as simulation predicted.

Index Terms — A. Stepped MOSCAP; B. NFGM; C. Multi-level storage; D. Stepped control oxide; E. Non-volatile memory

I. INTRODUCTION

The importance of development of non-volatile memory devices has emerged as a need in mobile equipment and portable memory drives. For non-volatile memory technology to meet its increased demands in the electronic industry, multi-level storage capability is needed to keep up an increasing degree of integration without facing further scaling issues. Currently commercialized TANOS type flash memory adopts multi-level cell (MLC) technology. However, MLC technology is not still content able due to its low reliability, higher bit error ratio and reduced ensure cycles compared to SLC [1]. Furthermore, conventional NAND flash memory has a drawback of its high driving voltage. NFGM is able to reduce driving voltage because it uses direct tunneling as a charge trapping mechanism. Besides NFGM has the advantage of improved retention, programming/erase speed and endurance due to discrete trap-site [2-5]. Thus realization of multi-level storage on NFGM has been attempted with considerable effort in such ways that applying multi-layer nanocrystals [7-10] [16] or mixture of different types of nanocrystals [11]. As one of these efforts, a stepped NFGM MOSCAP structure Fig.1 has been studied recently [12].

Figure 1. Schematic of a stepped NFGM MOSCAP structure.

A stepped NFGM MOSCAP realizes multi-level storage characteristics by the control of electric field intensity on the tunneling oxide through different thicknesses of the control oxide under a single gate electrode. This method requires only a simple additional etching process to the conventional NFGM processes. For proper control of the storage characteristics in a stepped NFGM MOSCAP, understating of structural parameters in relation with electrical properties is necessary. In this work, the way to predict the storage characteristic of a stepped NFGM MOSCAP structure was studied in terms of the control oxide thickness design. The simulation result was confirmed by the fabrication of a 40/20nm stepped capacitor consisting of Au nanocrystals.
II. EXPERIMENTAL PROCEDURE

After RCA cleaning and removal of native oxides from the Si substrate, 5nm of thermal SiO$_2$ was grown by dry oxidation to be used as a tunneling oxide. Then an Au nanocrystal array was formed on the SiO$_2$ by rapid thermal annealing (RTA) of Au wetting layer that was deposited by thermal evaporator. The thickness of the Au wetting layer was 1nm, and annealing was carried out at 500°C for 1min in N$_2$ ambient. Au nanocrystal was selected as the nano floating gate for its high work function. A metal nanocrystal composed with high work function material can create a NFGM exhibit with good retention characteristics for its deep effective well depth [3-4] [13-14].

Then HfO$_2$ was deposited on the Au nanocrystal array by atomic layer deposition (ALD) as a control oxide. 20nm thick and 40nm thick control oxide samples were prepared separately. Finally Al 100nm was deposited as top electrode by thermal evaporator. The electrode size was 100μm x 100μm.

Characteristics of these reference samples were measured by C-V measurement with a counter clockwise sweep. Prediction of storage characteristics of a stepped MOSCAP structure was evaluated from the pair of NFGM MOSCAP structures with two different control oxide thicknesses in parallel connection as described in Fig. 2. Finally, the stepped NFGM was fabricated by partial dry etching of 40nm control oxide using ICP dry etcher. The etch depth was controlled to be 20nm following the simulation result.

![Figure 2. C-V measurement of NFGM MOSCAP structures with different thicknesses in parallel connection.](image)

III. RESULT AND DISCUSSION

3.1 Width of memory window

From $V=Q/C$, the width of memory window can be expressed as

$$\Delta V_{TH} = \frac{t_{CO}}{\epsilon_{CO}}$$

(1)

Where, $\Delta V_{TH}$ is a threshold voltage shift and $Q$ is a real density of trapped charge [13] which can be determined from the density product of the nanocrystal array and the number of trapped charges in each nanocrystal particle. $t_{CO}$ and $\epsilon_{CO}$ represent thickness and dielectric permittivity of the control oxide, respectively. The number of trapped charges in one particle can be calculated as follows. When an electron is going to be trapped in a particle, it receives Coulombic repulsion from electrons which already exist in the particle. The strength of this effect is the charging energy

$$\Delta E = \frac{e^2}{C}$$

(2)

In this equation, C is capacitance of a particle[14] which is $4\pi r_{CO}$ assuming a sphere. Thus maximum number of electrons that can be trapped in an effective potential well of single particle is estimated as

$$n = \frac{d_{eff}}{\Delta E}$$

(3)

where $d_{eff}$ is an effective well depth of the particle which is 0.89eV in case of Au [15].
Thus, maximum memory window width in a capacitor with a particle density of \( n_{nc} \) can be calculated as

\[
\Delta V_{TH} = \left( \frac{t_{CO} \Delta N_{nc}}{\varepsilon_{CO}} \right) \left( \frac{d_{eff}}{\Delta E} \right) = \left( \frac{t_{CO} \Delta N_{nc}}{\varepsilon_{CO}} \right) \left( \frac{d_{eff}}{q/N_{eff}} \right)
\]  

(4)

### 3.2 Control oxide thickness dependency of storage characteristic

The effect of control oxide thickness variation on the storage characteristic of NFGM can be estimated. Applied voltage on the gate can be expressed in terms of the physical parameters of tunneling and control oxides.

\[
V = E_{TO} \left( \varepsilon_{TO} + \frac{\varepsilon_{TO} t_{TO}}{\varepsilon_{CO} t_{CO}} \right)
\]  

(5)

Where, \( E_{TO} \) is the electric field induced to tunneling oxide; \( t_{TO} \) and \( t_{CO} \) are thickness of tunneling oxide and control oxide; \( \varepsilon_{TO} \) and \( \varepsilon_{CO} \) are dielectric permittivity of tunneling oxide and control oxide, respectively. So the relative voltage \( V' \) applied to the control oxide with thickness \( t'_{CO} \) is given by

\[
V' = \left( \frac{t_{TO} + \varepsilon_{TO} t_{TO} t'_{CO}}{\varepsilon_{TO} + \varepsilon_{TO} t_{TO} t'_{CO}} \right) V
\]  

(6)

Since the memory window width is proportional to the control oxide thickness, one can predict memory window of NFGM MOSCAP by its control oxide thickness as plotted in Fig. 4 for the case of HfO\(_2\).
In addition, Fig. 4 suggests that the saturation voltage of the thinner oxide should be lower than the onset voltage of trapping through thicker oxide when we design a multi-level NFGM. Therefore, realization of two distinctive storage states is more favorable if the step height is larger. In this experiment, we selected a pair of 20nm and 40nm HfO$_2$ control oxides.

3.3 Parallel connection measurement of two capacitors with different control oxide thickness.

Fig. 5 is the result of C-V measurement of 20nm and 40nm thick capacitors in parallel connection. Step-shape C-V curve is associated with the overlap of two different C-V curves having different size of memory window. For example, the capacitance at the step shown in the voltage ranged from 3V to 6V is a result from the accumulation of the thick control oxide and the inversion of the thin control oxide. In addition, the step appears due to the larger memory window of the thick control oxide.

![Figure 5. C-V curves of 20 and 40nm NFGM MOSCAP structures in parallel connection. It shows step-shape C-V curves of multi-level storage characteristic.](image)

3.4 Stepped NFGM

In order to demonstrate the multi-level storage behavior in the stepped control oxide NFGM MOSCAP structure, we fabricated a stepped capacitor structure. Fig. 6 (a) shows TEM cross-sectional view of partially etched control oxide and Au nanocrystals. As we designed, the step height in the figure is close to 20nm. The plan view of Au nanocrystals is also presented in Fig. 6 (b). The average diameter and the density turn out to be 4.8nm and $1.8 \times 10^{12}$ cm$^{-2}$, respectively.

![Figure 6. (a) TEM cross-sectional view of stepped NFGM MOSCAP structure (b) TEM plan view of Au nanocrystals with an average diameter of 4.8nm and a density of $1.8 \times 10^{12}$ cm$^{-2}$.](image)

The C-V curve from the aforementioned stepped NFGM MOSCAP structure is shown in Fig. 7. At lower voltage the electric field is not strong enough to induce the electron tunneling, and results in no shift in C-V curve. As applied bias increases, the
C-V hysteresis begins to appear. Furthermore, the step-shape curves are shown in the region where the thinner control oxide is fully trapped and the thicker control oxide keeps on trapping charges in the 20/40nm stepped control oxide. The memory window can be estimated from Eq. (4). It is noticed from the equation that the memory window is only proportional to the oxide thickness when the nanocrystal size and the density are fixed. In the ideal case of 20nm and 40 nm thick component oxides, the respective memory windows are 8V and 16V. In Fig. 7, one can find the memory window follows the predicted values. The inner width between steps, which is approximately 8V, is thought as a memory window of the thinner control oxide, while the wide width around 14V is considered to be the saturated memory window. This amount of flat band voltage shift, 14V, is similar to the predicted value of 16V.

In order to realize distinguishable multi-level storage characteristics in a stepped NFGM MOSCAP structure, selection of low-k control oxide is advantageous. The low-k control oxide can increase the on-set of the second trapping voltage as inferred from $\epsilon_{CO}$ term in Eq. (5). However, tunneling becomes ineffective because the low-k control oxide layer can take up most of the applied voltage. In addition, smaller nanocrystal size or density is favorable to exhibit multi-level storage behavior according to Eq. (4). As the particle size or particle density becomes smaller, the interval between on-set and saturation voltage also becomes smaller and more distinct storage states can be realized, but the memory window shrinks. Since there is a trade-off between the two effects, judicious decision is necessary.

IV. CONCLUSION

In this work, multi-level storage characteristic in a stepped MOSCAP structure was predicted from the simple calculation. The simulation result can provide ideas about design of step height, memory window, on-set voltage of the first or the second trapping and saturation voltage, etc. Not only the thickness of thin and thick oxides in a step is important but also the dielectric permittivity of the control oxide turns out to affect the storage characteristics significantly. The storage properties of a 20/40nm stepped NFGM MOSCAP structure were estimated from parallel connection of a pair of step-free two capacitors of 20nm and 40nm thick control oxides. The measured data showed good match with the calculated values. As predicted in preliminary experiments, 20nm height stepped NFGM MOSCAP structure fabricated by partial etching of 40nm thick control oxide exhibited the multi-level storage characteristics. The memory window width also agreed well with the prediction suggesting one can easily double the storage capacity in conventional step-free NFGM by adding simple etching process.

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