Characteristics of various instability in Ni-FALC poly-Si thin film transistors

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In this study, the characteristics of positive bias temperature instability (PBTI) and cyclic constant voltage stress (CVS) in thin film transistors (TFTs) incorporating Ni-FALC poly-Si film were investigated under various stress conditions. In PBTI, the threshold voltage \( V_{TH} \) was degraded by a vertical electric field on the gate stack, and an abrupt variation of \( V_{TH} \) was attributed to the creation of defects in the gate oxide and the increase of the effective interface trap state. In contrast to the formation of defects, the poly-Si film was not sensitive to PBTI stress (the fluctuation in the grain boundary trap density was just 5.6%). In two-cycle CVS of devices before and after O2 plasma treatment, the direction of the \( V_{TH} \) shift and polarity of bias showed good correlation. In particular, the O2 plasma-treated device demonstrated low Subthreshold swing (S.S) and low minimum drain current compared to the untreated one. The improvement of device performance seemed to originate from the reduction of effective interface trap sites and leakage current paths.

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1. Introduction

Low-temperature polycrystalline silicon thin film transistors (LTPS–TFTs) have been widely used as driving elements in active matrix organic light emitting displays (AMOLED) as a circuit device for System-On-Glass (SOG) due to their high field effect mobility \( \mu \) [1,2]. However, because of the existence of intra-grain defects and grain boundaries, the performance of LTPS–TFTs can be significantly degraded by thermal stress, gate bias stress, and hot carrier stress. Moreover, it is well known that poly-Si TFTs have unstable characteristics under gate bias stress, such as large leakage current and degradation of device parameters due to grain-boundary-trapped Ni and effective interface trap density [3,4]. Furthermore, the quality of the gate dielectric and poly-Si/gate oxide interface plays an important role in determining the performance and endurance of TFTs [5]. The practical reliability of poly-Si TFTs remains an important issue.

In this study, the transistor characteristics of positive bias temperature instability (PBTI) and cyclic constant voltage stress (CVS) instability of Ni-FALC-processed poly-Si TFTs were investigated. In addition, O2 plasma treatment was employed to investigate the gate passivation effect of treatment on device characteristics under cyclic CVS. The quality of Ni-FALC-processed poly-Si channels is determined by factors such as metal-catalysts, thermal energy (annealing), and electric driving force (wind effect) [6]. Since the poly-Si channels obtained by Ni-FALC are superior to the poly-Si channels yielded by other thermal methods in terms of the minimization of metal residue in the channel region and directional crystallization [7], we wanted to evaluate the reliability of the devices under various stress conditions.

2. Experiment

A 50-nm-thick undoped a-Si layer was deposited on SiO2 passivated glass, and the active regions were defined by a typical photolithography method and reactive ion etching. The channel region in the active layer was then masked by a 60-nm-thick oxide layer. A 1.5-nm-thick Ni layer was deposited by the sputtering method on the source and drain region, followed by self-aligned plasma doping with 10 kV P ions. For uniform crystallization by the FALC process, where an identical electric current has to be supplied to every a-Si channel in a pixel transistor array, metal lines connecting sources and drains were formed from metal (Mo) deposition and patterning. After crystallization of the a-Si layer at 500 °C for 4 h in ambient nitrogen with an electrical driving force (electric current), the metal lines and sacrificial oxide layer on the gate area were removed by wet etching. Low temperature deposition of a 100-nm-thick SiO2 film as the gate dielectric was carried out by plasma-enhanced chemical vapor deposition (PECVD) at 280 °C and patterned sequentially by dry etching and wet etching.
The channel length and width/length ratio were 20 μm and 1:1, respectively. The threshold voltage was determined by the constant current method (at 100 nA × W/L, V_DS = 0.1 V) [8]. The transfer characteristics of Ni-FALC poly-Si TFTs were measured at V_DS = 0.1 V and V_G = −5−15 V. The two PBTI stresses were set at V_G − V_{TH} = 15 V (PBTIA) and V_G − V_{TH} = 25 V (PBTIB), with the other terminal connected to the ground for 7000 s at T = 25 °C and T = 85 °C. For one cycle of CVS conditions, a positive gate voltage was applied for 1000 s (PBTI) and then the reversed polarity of the gate voltage was applied for 1000 s (relaxation). In total, it took 4000 s to examine the threshold voltage shift (ΔV_{TH}) under two-cycle CVS at a stress temperature of 100 °C. All measurements were performed in dark conditions using an Agilent 5270B semiconductor parameters analyzer. For the investigation of interface passivation effects after treatment in TFTs under cyclic CVS, we carried out conventional O2 plasma treatment at 35 mtorr, 20 W for 5 min.

3. Results and discussion

Fig. 1 shows the I_D–V_G characteristics of Ni-FALC-processed TFT before and after 1000 s PBTI stress at 25 °C and 85 °C. Device parameters extracted from the transfer curve under various PBTI stresses are summarized in Table 1. The values show degradation in minimum drain current (I_{MIN}) from 2.12 pA to 6.14 pA and S.S from 0.8 V decade$^{-1}$ to 1.8 V decade$^{-1}$ with an increase in stress time and vertical electric field strength. In addition, degradation of the device at 85 °C showed a similar tendency at 25 °C. The difference between the stressed device at 25 °C and 85 °C was simply the direction of the threshold voltage shift compared to the fresh one. In the former, threshold voltage (V_{TH}) changed toward a positive direction by trapping electrons in the oxide [9], while, in the latter, V_{TH} changed toward a negative direction. This difference may be associated with the increase of conductance (G) due to the increase of thermally activated carrier concentration. However, the V_{TH} of both devices (25 °C, 85 °C) shifted toward a positive direction under PBTI stress. According to a review by Toshiharu Suzuki [2], I_{MIN} and S.S are influenced by grain boundary trap density (N_{GB}) and the effective interface trap state density of the poly-Si and gate dielectric/poly-Si interface. To estimate N_{GB} and effective trap density (D_{it}) near the SiO_2/poly-Si interface, we adopted the methods reported by both Proano et al. and Levinson et al. [10,11], and a method that can be calculated from the S.S by neglecting depletion capacitance in the channel layer [12], respectively. At 25 °C, N_{GB} and D_{it} were degraded from 2.52 × 10^{12} cm$^{-2}$ to 7.77 × 10^{12} cm$^{-2}$ and from 2.4 × 10^{12} cm$^{-2}$ to 6.52 × 10^{12} cm$^{-2}$, respectively, with an increase of stress time and electric field strength (Table 1).

In the stressed device at 85 °C, these values increased from 1.35 × 10^{12} cm$^{-2}$ to 4.19 × 10^{12} cm$^{-2}$ and from 1.89 × 10^{12} cm$^{-2}$ to 2.43 × 10^{12} cm$^{-2}$, respectively. Such a result confirms a correlation between the tendency of the trap density and I_{MIN} or S.S. In addition, defect sites (grain boundary trap density, gate dielectric/poly-Si interface trap site) of the device stressed for 1000 s decreased with the reduction of stress time and strength of the electric field and increased with a decrease in temperature. In general, the device sheet conductance (G) depends on temperature through the variation of thermally activated carrier concentration [13].

The PBTI stresses were applied to the gate electrode at 25 °C and 85 °C for 7000 s in order to investigate the long-term threshold voltage shift (ΔV_{TH}) of the TFT. The threshold voltage shift was defined as ΔV_{TH} = V_{TH}(t) − V_{TH}(t = 0). In general, ΔV_{TH} is determined by the following factors: charges trapped in the gate dielectric; interface deep state generation; trap state creation in the gain boundary; and intra-grain [4], weak Si–Si, and Si–H bonds [14]. The ΔV_{TH} in present study is shown in Fig. 2. Both PBTIA cases (T = 25 °C, 85 °C) showed similar behavior in ΔV_{TH} up to 1000 s. However, the V_{TH} at 85 °C shifted abruptly after a stress of 1000 s, possibly related to the creation of new defect sites in the gate dielectric or SiO_2/poly-Si interface.

Fig. 3 shows the gate leakage current of TFT under PBTIA stress conditions at 85 °C. When PBTIA stress time was 3000 s, a large increase in gate leakage current resulted from the creation of new trap sites in the gate dielectric and gate dielectric/poly-Si interface. For confirmation, we calculated the N_{GB} and D_{it} before and after 3000 s of PBTIA at 85 °C. The N_{GB} and D_{it} of TFT under PBTIA (1000 s) were 1.35 × 10^{12} cm$^{-2}$ and 1.89 × 10^{12} cm$^{-2}$, respectively. These values changed to 1.43 × 10^{12} cm$^{-2}$ and 4.27 × 10^{12} cm$^{-2}$, respectively, for PBTIA for 3000 s. The change in N_{GB} of only 5.9% suggests that such a significant threshold voltage shift can be

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**Table 1** Summary of the device parameters of Ni-FALC poly-Si TFTs before and after 1000 s of PBTI.

<table>
<thead>
<tr>
<th>Stress condition</th>
<th>V_{TH} (V)</th>
<th>S-factor (V decade$^{-1}$)</th>
<th>N_{GB} (10^{12} cm$^{-2}$)</th>
<th>D_{it} (10^{12} cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-stress</td>
<td>4.6</td>
<td>0.8</td>
<td>2.92</td>
<td>2.4</td>
</tr>
<tr>
<td>PBTIA (25 °C)</td>
<td>4.6</td>
<td>0.85</td>
<td>4.1</td>
<td>2.96</td>
</tr>
<tr>
<td>PBTIB (25 °C)</td>
<td>5.2</td>
<td>1.8</td>
<td>7.77</td>
<td>6.52</td>
</tr>
<tr>
<td>PBTIA (85 °C)</td>
<td>3.0</td>
<td>0.85</td>
<td>1.35</td>
<td>1.89</td>
</tr>
<tr>
<td>PBTIB (85 °C)</td>
<td>3.4</td>
<td>1.0</td>
<td>4.19</td>
<td>2.43</td>
</tr>
</tbody>
</table>

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Fig. 1. Transfer characteristics of Ni-FALC poly-Si TFTs before and after 1000 s of PBTI at temperature stresses of 25 °C and 85 °C.

Fig. 2. Threshold voltage shift (ΔV_{TH}) of Ni-FALC poly-Si TFTs under PBTI stress at temperature stresses of (a) 25 °C and (b) 85 °C.

A 300-nm-thick Mo gate electrode and source/drain pad was then formed.
explained by the creation of bulk defects and the increase of interface trap sites. In addition, $N_{\text{LT}}$ did not change much before and after 3000 s of PBTIA stress at 85 °C, implying that there was no noticeable degradation of poly-Si quality induced by PBTIA stress. From the $\Delta V_{\text{TH}}$ of TFTs under other stress conditions, it appears that the creation of a trap state in the gate dielectric and interface is likely responsible for the large $\Delta V_{\text{TH}}$. To investigate the cyclic CVS instability of the devices, an electrical bias was applied to the gate electrode at a temperature of 100 °C.

$\Delta V_{\text{TH}}$ revealed a good correlation between the direction of the $V_{\text{TH}}$ shift and bias polarity. In addition, the $\Delta V_{\text{TH}}$ of the O2 plasma-treated TFT was smaller than the $\Delta V_{\text{TH}}$ of the untreated TFT. When the stress reached 220 s, the $\Delta V_{\text{TH}}$ difference between the two samples was 0.41 V. However, $V_{\text{TH}}$ relaxation of the untreated TFT was more effective than that of the treated device. This effect may be associated with the passivation of the interface between SiO2 and poly-Si by the O2 plasma treatment. For the sake of a more quantitative understanding of this passivation effect, we calculated S.S and $D_{\text{fi}}$.

Fig. 5 shows the variation of S.S and $D_{\text{fi}}$ in the two devices during one-cycle CVS (stress-relaxation). When the stress ($V_{\text{G}} = 20$ V) approached 220 s, the S.S on the two devices improved from 0.63 V decade$^{-1}$ to 0.43 V decade$^{-1}$ ($\Delta S.S = -0.2$ V decade$^{-1}$) and from $2.14 \times 10^{12}$ cm$^{-2}$ to $1.08 \times 10^{12}$ cm$^{-2}$ ($\Delta V_{\text{TH}} = -1.06 \times 10^{12}$ cm$^{-2}$), respectively. S.S was determined by the effective $D_{\text{fi}}$ according to the report by C. A. Dimitriadis et al. [12]. The variation of S.S and $D_{\text{fi}}$ displayed in Fig. 5 confirms that the O2 plasma post-treatment effectively passivated the interface between the SiO2 and poly-Si channel thin film. In addition, the minimum drain current ($I_{\text{MIN}}$) was reduced from $1.52 \times 10^{-10}$ A to $5.57 \times 10^{-11}$ A after O2 plasma treatment. This decline was attributed to several factors, including a reduction of gate leakage current, reduction of the junction leakage current at the drain side, and curing of the leakage current path generated during the plasma etching of gate oxide, among others [15].

4. Conclusions

We investigated the characteristics of PBTI and the cyclic CVS instability of Ni-FALC poly-Si TFTs. A large $V_{\text{TH}}$ shift under PBTI was observed that seemed to be related to defect formation in the gate dielectric, leading to an increase of $D_{\text{fi}}$. In two-cycle CVS tests, the $\Delta V_{\text{TH}}$ and $I_{\text{MIN}}$ of O2 plasma-treated devices were smaller than for untreated devices. This difference may be attributed to the reduction of interface traps and curing of the leakage current path at the edge of the gate stack. The FALC process is an effective way to obtain high quality poly-Si with good endurance and performance in LTPS--TFTs.

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