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Electrical characteristics of polycrystalline silicon thin film transistors using the Cu-field aided lateral crystallization process

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Polycrystalline silicon thin film transistors (poly-Si TFTs) were fabricated on glass substrate by using a concept of Cu-field aided lateral crystallization (Cu-FALC). The crystallization of a-Si was significantly enhanced when an electric field of 30 V/cm was applied to selectively Cu-deposited amorphous silicon (a-Si) film during thermal annealing at 500 °C for 3 h. These FALC TFTs using Cu exhibited a low off-state leakage current of $6.2 \times 10^{-12}$ A at $V_g = -10$ V and a maximum on/off current ratio of $3.1 \times 10^5$. The field-effect mobility and the threshold voltage of the fabricated poly-Si TFT were about 22.0 cm$^2$/V s and 3.9 V, respectively. Therefore, the possibility of high-performance and low-temperature ($<500$ °C) poly-Si TFTs was demonstrated by using Cu-FALC technology. © 2002 American Vacuum Society. [DOI: 10.1116/1.1491552]

I. INTRODUCTION

Polycrystalline silicon thin film transistors (poly-Si TFTs) with higher mobility have been pursued aggressively due to their potential applications in fully integrated driver circuits and pixel switching transistors on the same glass substrate.\(^1\) In spite of many advantages of poly-Si TFTs, some problems, such as lowering the crystallization temperature and decreasing the leakage current density in the off state, have to be resolved.\(^2,3\) Up to now, in the cases of crystallization proposed to form poly-Si, metal induced crystallization (MIC) has been known as a lower temperature process alternative to solid phase crystallization.\(^4\) However, it is difficult to fabricate poly-Si TFT using the MIC process because it has a serious shortcoming in the undesirable incorporation of metal impurities in the channel region of the transistor. Further, poly-TFTs fabricated by using the metal-induced lateral crystallization (MILC) process have been reported. This crystallization initiated by the MIC process propagates to the metal-free region during annealing.\(^5,6\) Nevertheless, in this method, the metal silicide phase which acts as a source to the detriment of electrical characteristics can remain at the center region of the transistor channel because the crystallization velocity from the metal deposited region on the source and drain regions is the same in all directions. Considering the above, MIC and MILC processes are not the best solutions for poly-Si TFT fabrication in terms of the productivity and quality of the film.

In previous work, we proposed a crystallization process, field aided lateral crystallization (FALC), in which an electric field was applied during the crystallization. The crystallization velocity was increased and the crystallization time was shortened.\(^7,8\) Moreover, we have investigated the FALC characteristics and could successfully fabricate the poly-Si TFT using Ni-FALC below 500 °C.\(^8,9\) In addition, we have applied Cu to the FALC process and as a result, Cu was found to induce the lateral crystallization at low temperature ($<500$ °C) under the influence of the electric field and the velocity of Cu-FALC was faster than that of Ni-FALC.\(^10\) Despite these favorable properties, Cu exhibits a higher diffusivity in silicon and has a very high tendency to precipitate during the cooling of the thermal cycle and even at room temperature.\(^11\) Cu precipitates formed at the SiO$_2$/Si interface during the FALC process could lead to localized thinning of gate oxide. Therefore, it could degrade gate oxide integrity causing breakdown and junction leakage current.

In this study, we proposed a new TFT fabrication method in which the TFT channel region is crystallized by the Cu FALC process before the definition of gate structure on the active layer. We also tried to crystallize the channel length as larger than the gate length to see whether this method would show an effect on the off-set process as shown in Fig. 1(b). That is, the interface region of MIC/FALC is located outside of the gate junction region. Moreover, the activation process after the ion mass doping (IMD) process was performed by using the eximer laser annealing (ELA) system to shorten thermal processing time. Besides, it might prevent copper silicides from diffusing into the gate oxide by thermal diffusion during annealing and minimize metal residues near gate oxide.

II. EXPERIMENT

The schematic cross section of the proposed Cu-FALC TFT is presented in Fig. 1. A 500-Å-thick a-Si film was deposited on the glass substrate by plasma enhanced chemical vapor deposition at 430 °C using SiH$_4$ and H$_2$ as source gases. The Cu-FALC process for formation of poly-Si as an active layer of the transistor is shown in Fig. 1(a). After rectangular-shaped photoresist (PR) patterns on a-Si were formed by the photolithography process, a 20-Å-thick Cu was deposited using the dc sputtering system. Then, the Cu layer on the PR pattern was lifted off and the rectangular-shaped Cu-free patterns were left. The electric field was applied to the specimen by a dc power supply through the

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electrodes formed on two opposite sides of the substrates during crystallization. The crystallization process was performed at 500 °C for 3 h with an electric field of 30 V/cm in N2 ambient. For the gate structure, a SiO2 gate dielectric (1000 Å) was deposited by rf magnetron sputter and the Mo gate electrode (3000 Å) deposition using dc magnetron sputter. As shown in Fig. 1 (b), the metal gate was defined by reactive ion etching using SF6 and O2 plasma and the gate oxide was etched by diluted HF solution using the Mo gate as a mask. IMD of PH3 gas was carried out at room temperature with an acceleration voltage of 10 kV. Under these conditions, the ion dose was fixed at 1 × 1015 cm−2. The dopant activation process was accomplished by ELA at room temperature. The laser energy density used in the activation process was 224 mJ/cm2 per pulse with an acceleration voltage of 27 kV. Finally, Al electrodes were formed and the alloying was done at 350 °C for 30 min in N2 ambient. The electrical characteristics of current versus voltage for fabricated transistors were measured by the HP4140B system. After the specimen was annealed, the crystallization behaviors in every pattern were observed by Nomarski optical microscopy and the degree of crystallization was investigated by micro-Raman spectroscopy. The microstructure of the crystallized region was examined by a scanning electron microscopy (SEM).

III. RESULTS AND DISCUSSION

The Nomarski optical micrograph of partially crystallized a-Si using Cu at 500 °C for 3 h with an electric field of 30 V/cm is shown in Fig. 2. During the annealing, a-Si in the T-shaped pattern was laterally crystallized from the negative electrode side to the positive electrode, which exhibited a typical FALC aspect. The outside T-shaped pattern is originally the a-Si film directly in contact with Cu. The low temperature crystallization initiates from this region and propagates into the inside metal-free T-shaped region by an electric field-assisted thermal diffusion of the copper silicide phase. The crystallization velocity of Cu-FALC in the T-shaped pattern is about 18 μm/h.

In order to investigate the degree of crystallization of poly-Si crystallized by Cu-FALC, a Raman beam was focused on the crystallized region inside the (A region) T-shaped pattern as shown in Fig. 3. Single crystalline silicon (c-Si) has a sharp peak around 520 cm−1 in Raman spectra. The intensity of Raman spectra measured from the crystallized region by Cu-FALC does not reach the intensity from single c-Si but it shows obvious evidence of crystallization. On the other hand, the uncrystallized a-Si region inside (B region) of the T-shaped pattern shows a broad peak around 480 cm−1, which is a typical characteristic peak of a-Si in Raman spectra. From these results, it was identified that Cu induced the lateral crystallization under the electric field.

Figure 4 shows the SEM images of the microstructure of a-Si film crystallized through Cu-FALC by an electric field of 30 V/cm at 500 °C. The left-hand side in Fig. 4 (a) shows the region crystallized by the Cu-FALC process. The lateral
crystallization in the T-shaped pattern seems to progress noticeably from the negative electrode side toward the positive electrode side under the applied electric field. Although each protrusion did not grow uniformly, the protrusions grew totally toward the \textit{a}-Si region. The diameter of the grains appears to be 30–50 nm and the grain size of poly-Si was fairly uniform as shown in Fig. 4\textit{a} and \textit{b}.

Therefore, the electrical characteristics of TFTs formed anywhere on the active layer would result in uniform property.

Generally, it is known that the poly-Si TFTs fabricated by conventional MIC or MILC processes have defects in the channel region of the transistor. In particular, Cu diffuses very fast into the gate oxide and degrades the dielectric property of the gate oxide. The Cu precipitates formed at the SiO$_2$/Si interface during annealing lead to localized thinning of gate oxide and enhances the local fields in the vicinity of the precipitates. It might increase the leakage current in the off state by inducing the current injection in spite of a lower applied voltage. Therefore, we tried to fabricate FALC TFT using a process which could minimize the incorporation of the metal contaminants near the gate structure and metal diffusion into the gate oxide. Several modifications of the process are as follows. First, the Cu-FALC process was performed before the deposition of gate oxide to avoid the chance for Cu to diffuse into the oxide layer during the crystallization. Second, we made the channel length larger than the gate length on the active layer to place the interface region of MIC/FALC outside of the gate junction region through a lithography technique [Fig. 1\textit{b}]. Third, the activation of drain and source was performed using ELA to minimize the Cu diffusion by shortening the thermal processing time.

Figure 5 shows the drain current ($I_{ds}$)–gate voltage ($V_{gs}$) characteristics of Cu-FALC TFT at $V_{ds}$ (drain voltage) = 0.1 V. FALC TFT using Cu shows relatively superior properties.

![FIG. 4. SEM images of crystallized microstructure using Cu-FALC](image)

![FIG. 5. Current–voltage characteristics of poly-Si TFT fabricated using Cu-FALC](image)

<table>
<thead>
<tr>
<th>TABLE I. Device parameters of poly-Si TFT fabricated by the Cu-FALC process. The data of Ni-FALC TFT are also listed.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu-FALC TFT</td>
</tr>
<tr>
<td>$N$-channel, $V_g$=0.1 V, $500 \degree C$, 3 h, $E=30$ V/cm</td>
</tr>
<tr>
<td>Width/length ($\mu m$)</td>
</tr>
<tr>
<td>Threshold voltage (V)</td>
</tr>
<tr>
<td>Field effect mobility (cm$^2$/V s)</td>
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<tr>
<td>Maximum on/off current ratio</td>
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<td>Leakage current (A) at $V_g$=–10 V</td>
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compared with the previously suggested characteristics of TFTs fabricated using the Cu solution, as summarized in Table 1. In particular, the leakage current ($6.2 \times 10^{-12}$ A) at $V_g = -10$ V decreased by about 1 order. It can be judged that such differences in the transistor characteristics depend mainly on the concentration of impurity at the junction region near the gate on the active layer. It is reported that the leakage current at high drain voltage and the high negative gate voltage might come from the field-enhanced tunneling of electrons in the valance band to the conduction band via grain boundary traps in the case where the metal layer is deposited in the drain region. The field-effect mobility of FALC processed TFTs was increased relatively due to the minimization of metal residues in the channel region by the FALC process and the threshold voltage was lowered. The measured data are shown in Table I and for comparison, the previous data of Ni-FALC TFT are also included in Table I.

Consequently, the proposed Cu-FALC TFT fabrication process could enhance the electrical properties of poly-Si TFTs.

IV. CONCLUSION

Poly-Si TFTs adopting the Cu-FALC process were fabricated by applying an electric field of 30 V/cm at 500 °C. Through some modifications of the conventional FALC process steps to reduce the contamination of a relatively fast diffusing crystallization mediator, Cu, the reasonably good properties of poly-Si TFTs could be obtained. By minimizing Cu residues near the gate region and in the channel region, the off-state leakage current was reduced to $6.2 \times 10^{-12}$ A at $V_g = -10$ V. This lower leakage current is attributed to the fact that the junction quality near the gate was improved by the fabrication process of FALC TFT and that the gate oxide quality was enhanced due to the minimization of Cu diffusion into the gate oxide. The field-effect mobility and the threshold voltage were about 22.0 cm$^2$/V s and 3.9 V, respectively. Therefore, we confirmed the possibility of low temperature (<500 °C) poly-Si TFT by using Cu-FALC technology.

ACKNOWLEDGMENT

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